REMARKS

The Office Action of January 25, 2006 was received and reviewed. Applicants would like to thank the Examiner for the consideration given to the above-identified application.

Reconsideration and withdrawal of the currently pending rejections are requested for the reasons advanced in detail below.

Claims 1-25 are pending prior to the instant amendment for consideration, of which claims 1, 2, 4, 5 and 7 are independent. By this amendment, claims 1-20 have been amended. Claims 26-36 have been withdrawn from consideration. Consequently, claims 1-25 are currently pending for consideration in the instant application.

Referring now to the detailed Office Action, claims 1, 16 and 21 stand rejected under 35 U.S.C. §102(e) as being anticipated by Nakamura et al. (U.S. Patent No. 6,887,724 – hereafter Nakamura). Further, claims 2-6, 11-14, 17-19 and 22-24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Nakamura in view of Nishimura et al. (U.S. Patent No. 6,462,802 – hereafter Nishimura). Finally, claims 7-10, 15, 20 and 25 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Nakamura and Nishimura and further in view of Fujikawa et al. (U.S. Patent No. 6,836,140 – hereafter Fujikawa). These rejections are respectfully traversed at least for the reasons provided below.

The presently claimed invention, as recited in amended independent claims 1, 2, 4, 5 and 7, includes, among other features, a semiconductor film which is formed to have a low concentration impurity region overlapping the gate electrode (e.g., element 208), and a step of measuring resistance of the low concentration impurity region of the TEG (Test Element Group). An object of the present invention is to form a TEG for measuring an impurity concentration of a gate-overlapped region, as disclosed on page 4, lines 8-11, (i.e., paragraph [0014] of the substitute specification submitted July 27, 2004).

On the other hand, Nakamura does not disclose Applicants' claimed features as alleged by the Examiner. Instead, Nakamura discloses forming an LDD region having a lower impurity concentration than that of the source and drain regions in the actual panel, as shown column 4, lines 65-57, column 5, lines 1-2. As such, it appears that Nakamura fails to teach, disclose or suggest a semiconductor film which is formed to have a low concentration impurity region overlapping the gate electrode and a step of measuring resistance of the low concentration impurity region (overlapping the gate electrode) of the TEG, as recited in

Applicants' pending claims.

Consequently, since each and every feature of the present claims is not taught (and is not inherent) in the teachings of Nakamura, as is required by MPEP Chapter 2131 in order to establish anticipation, the rejection of claims 1, 16 and 21, under 35 U.S.C. §102(e), as anticipated by Nakamura is improper.

With respect to the obviousness rejection of claims 2-6, 11-14, 17-19 and 22-24 over Nakamura and Nishimura, the Examiner relied on Nishimura as curing the deficiency of Nakamura, since Nishimura discloses a gate electrode that is laminated with a first conductive film and a second conductive film. With respect to the obviousness rejection of claims 7-10, 15, 20 and 25 over Nakamura, Nishimura and Fujikawa, the Examiner relied on Nishimura as curing the deficiency of Nakamura, since Nishimura discloses a gate electrode that is laminated with a first conductive film and a second conductive film, and the Examiner further relied on Fujikawa as disclosing a plurality of first to third TEGS. In response, Applicants respectfully note that one object of the present invention is to form a TEG for measuring an impurity concentration of a gate-overlapped region, as previously mentioned. The present invention discloses that a resistance distribution of a gate-overlapped region corresponding to a tapered shape of a gate electrode can be obtained by measuring sheet resistance of a Lov resistance monitor formed. This measurement cannot be obtained in a conventional manner (page 7, lines 11-13, or paragraph [0035] of the substitute specification submitted July 27, 2004).

Applicants respectfully assert that, as agued above with respect to the anticipatory rejection, Nakamura fails to teach, disclose or suggest a semiconductor film which is formed to have a low concentration impurity region overlapping the gate electrode and a step of measuring resistance of the low concentration impurity region (overlapping the gate electrode) of the TEG. Further, Applicants respectfully assert that it appears that Nishimura and Fujikawa also fail to teach, disclose or suggest these features. Therefore, the combination of Nakamura, Nishimura and Fujikawa is improper.

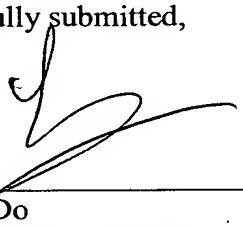
The requirements for establishing a *prima facie* case of obviousness, as detailed in MPEP § 2143 - 2143.03 (pages 2100-122 - 2100-136), are: first, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference to combine the teachings;

second, there must be a reasonable expectation of success; and, finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. As Nakamura, Nishimura and Fujikawa are deficient as discussed above, their combination in the obviousness rejections are improper and should be withdrawn.

Claims 1-20 have been amended, as shown above, to further improve and clarify the claim language.

In view of the foregoing, it is respectfully requested that the rejections of record be reconsidered and withdrawn by the Examiner, that claims 1-25 be allowed and that the application be passed to issue. If a conference would expedite prosecution of the instant application, the Examiner is hereby invited to telephone the undersigned to arrange such a conference.

Respectfully submitted,



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